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Design and Operation of Microelectrochemical Gates and Integrated Circuits

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Abstract: Here we report a simple design philosophy, based on the principles of bipolar electrochemistry, for the operation of microelectrochemical integrated circuits. The inputs for these systems are simple voltage sources, but because they do not require much power they could be activated by chemical or biological reactions. Device output is an optical signal arising from electrogenerated chemiluminescence. Individual microelectrochemical logic gates are described first, and then multiple logic circuits are integrated into a single microfluidic channel to yield an integrated circuit that can perform parallel logic functions. AND, OR, NOR, and NAND gates are described. Eventually, systems such as those described here could provide on-chip data processing functions for lab-on-a-chip devices.

Introduction

Here we report a simple approach for fabricating microelectrochemical integrated circuits (MICs), which are based on the principles of bipolar electrochemistry.[1] Individual microelectrochemical gates are able to perform basic logic functions, such as AND, OR, and NAND, but these gates can also be linked within a single microfluidic channel to perform parallel logic functions. The output state of these MICs is reported using electrogenerated chemiluminescence (ECL),[1,2] which generates an optical signal that can be easily detected using a CCD or even with the naked eye. Importantly, individual MICs are powered without wires and using just a single pair of driving electrodes that operate an arbitrarily large number of gates. The significance of MICs is that their logic operations depend on the state of faradaic electrochemical reactions present within microchannels, and therefore they provide a bridge between electronics and electrochemistry.

The challenge of signal processing and computation in microfluidic devices has become an active area of research as interest in microfluidics continues to expand. Rather than compete directly with the success of solid-state electronic processors, information processing in chemical or microfluidic systems[3,4] attempts to repurpose the concepts underlying solid-state processors and adapt them to chemical-based analysis.[5] By combining the advantages of computing systems with microfluidics, the functionality of small, high-density chemical devices may become more efficient and intelligent.[6,7]

Several examples of microfluidic-based logic gate designs have been reported. For example, Prakash and Gershenfeld used bubbles in multichannel microfluidic designs to demonstrate AND, OR, and NOT logic functions, a flip-flop device, a counter, an oscillator, and a modulator.[8] Here, the bubbles were "bit" information carriers, and bubble-to-bubble hydrodynamic interactions were used to control flow resistance in specific microchannels. Therefore, when the bubbles were injected as input signals, the paths of the bubbles through these devices were determined as a result of the changing flow resistances. The paths are the output of the logic operations, and the presence of the bubbles monitored at specific positions presented digital output signals.

Park and co-workers have also reported AND, XOR, and INH (inhibiting) logic gates that are based on chemical changes initiated by controlled mixing of reactants.[9] Their device consisted of two layers: the top layer contained a microfluidic mixer that accepted incoming chemical signals (for example, different pHs or metal ion concentrations), and the bottom layer contained valves that controlled the flow of the incoming fluids of the top layer. The logic functions were carried out by the fluidic plumbing of the bottom layer, and the output state was determined by the state of the mixed solutions in the top layer.

We previously reported electrochemical microfluidic logic gates, including OR and NAND gates, that used electroactive

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10.1021/ja107095z

chemicals as their inputs and ECL as the output.[10] In most cases these devices involved direct electrical connections to the input electrodes, but in some cases bipolar electrodes (BPEs) were used to transmit information between independent fluidic channels. The configuration used in these early experiments was quite different from the one described here, because now the BPEs are activated by the electric field present within the channel rather than by direct connections. As mentioned earlier, it is this advance, along with our finding that multiple BPEs may be used within a single fluidic channel without distorting the applied electric field,[11−13] that opens the possibility of large-scale, parallel processing systems.

The properties of BPEs relevant to the present study have been reported in several recent publications.[14−19] Briefly, redox reactions at a BPE are activated by a potential difference between each pole of the BPE and the solution. The electric field responsible for this potential difference is applied by a power supply connected to driving electrodes present in reservoirs situated at the ends of the fluidic channel.[14,15] Three aspects of BPEs are particularly relevant to the present study. First, many BPEs can be simultaneously activated using a single power supply and pair of driving electrodes.[12] Second, the electrochemical state (that is, whether or not current is flowing within a BPE) of an array of BPEs can be reported by ECL[13] or Ag electrodissolution.[11] The latter point is especially important, because direct current measurements in large arrays of BPEs would be unwieldy. Third, the current through a BPE can be directly measured using the split electrode design discussed later.[19]

In this report, we will first describe the behavior of BPEs that are under active potential control in a uniform electric field. These fundamental principles are used to demonstrate AND, OR, NAND, and NOR microelectrochemical logic gates. Multiple individual gates are then integrated within a single channel to show they can be simultaneously activated by a single electric field applied across the channel.

Experimental Section

Chemicals. The following chemicals were used as received unless otherwise noted in the text: $Ru(bpy)_3Cl_2 \cdot 6H_2O$ and tri-*n*-propylamine (TPrA) from Sigma-Aldrich (Milwaukee, WI). All solutions contained 2.0 mM $Ru(bpy)_3^{2+}$, 25.0 mM TPrA, and 0.10 M phosphate buffer (pH = 6.9). Milli-Q water (Milli-Q reagent water system, Millipore, Bedford, MA) was used to prepare all aqueous solutions.

Device Fabrication. The microchannels were prepared from poly(dimethylsiloxane) (PDMS) monoliths, and the BPEs were microfabricated Au wires supported on glass substrates and incorporating Cr adhesion layers. We have described the procedure for fabricating such devices previously,[19] but it is briefly summarized here. The PDMS channels were prepared from Sylgard 184 (Dow Corning, Midland, MI) by soft lithography.[20] The dimensions of the channel were 12.0 mm long, 1.0 mm wide, and 28 μm high. A 1.0 mm-diameter hole punch was used to form the reservoirs at the ends of the microchannel.

The logic gate electrodes were fabricated as 50 μm-wide microbands using appropriate mask designs on Au-coated glass slides (5 nm Cr adhesion layer and 100 nm Au layer, EMF Corp., Ithaca, NY). A layer of positive photoresist ($\sim$10 μm thick, AZ P4620) was spin-coated onto the glass slide and then exposed to UV light though a positive photomask containing the electrode design. These microstructures were then transferred to the Au slides after developing the photoresist (AZ 421 K, AZ Electronic Materials, Somerville, NJ) for 2 min and etching the Au and Cr layers. The Au layer was removed by immersion into an aqueous solution containing 5% I_2 and 10% KI (w/v) for 2 min, and the Cr adhesion layer was etched using an aqueous solution containing 9% $(NH_4)_2Ce(NO_3)_6$ (w/v) and 6% $HClO_4$ (v/v) for 30 s. Finally, the remaining photoresist was removed with acetone, and the slides were cleaned in piranha solution prior to assembly of the microfluidic device. (Warning: piranha solution is a strong oxidant, consisting of 30% H_2O_2 and 70% H_2SO_4 (v/v), that reacts violently with organic materials. It should be handled with extreme care, and all work should be performed under a fume hood and with protective gear.) The microfabricated slides and PDMS microchannels were treated with an air plasma for 15 s, and then they were pressed together with the BPEs situated at the center of the channel.

Logic Gate Operation. The inputs to the logic gates are independent and ungrounded voltages (InA and InB) applied to two pairs of microband electrodes using a dual-output power supply (E3620A, Agilent Technologies, Santa Clara, CA). The device output is an ECL signal at the reporting BPE. The electric field inside the microfluidic channel, which is responsible for activating the reporting BPE, is generated by applying 26.0 V across the channel using a power supply (Lambda LLS-9120, TDK-Lambda Americas Inc., San Diego, CA).

ECL output signals were detected by an optical microscope (Nikon AZ100, Nikon Co., Tokyo, Japan) equipped with a mercury lamp (Nikon) and a CCD camera (Cascade, Photometrics Ltd., Tucson, AZ). The ECL intensity profiles were obtained using V++ Precision Digital Imaging software (Digital Optics, Auckland, New Zealand). For consistency, the ECL reporting electrode is situated on the right side of each device.

Results and Discussion

Controlling the Response of BPEs by Applying Input Voltages. When a potential (E_{tot}) is applied across a microchannel that has been filled with an electrolyte solution (Scheme 1a), a uniform electric field (V_0) results in a linear potential gradient through the channel. Therefore, the potential difference ($\Delta E_{e\text{-field}}$) between any two points, separated by distance d, along the channel is described by eq 1.

$$\Delta E_{e\text{-field}} = V_0 d \tag{1}$$

When microbands separated by distance d are externally connected by a jumper wire, they form a split BPE, wherein each microband acts as either a cathodic or anodic pole (Scheme 1a).[19,21,22] The interfacial potential difference between the BPE and the solution is the sum of the anodic and cathodic interfacial

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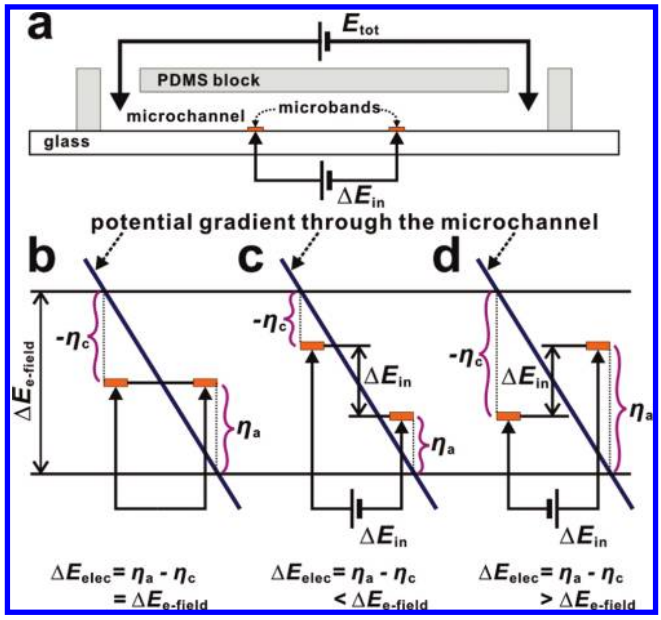
Scheme 1



overpotentials ($\Delta E_{elec} = \eta_a - \eta_c$) and in this case is equal to $\Delta E_{e\text{-field}}$ (Scheme 1b). Under these circumstances, we say that the BPE is in a passive mode, because ΔE_{elec} is determined exclusively by the externally applied, uniform electric field, V_0. However, when an auxiliary input voltage (ΔE_{in}) is applied between the microbands comprising the split BPE using an ungrounded power supply, $\Delta E_{e\text{-field}} = \eta_a - \eta_c + \Delta E_{in}$ (Scheme 1c and 1d). Thus, ΔE_{elec} can be described by eq 2.

$$\Delta E_{elec} = \eta_a - \eta_c = \Delta E_{e\text{-field}} - \Delta E_{in} \quad (2)$$

In this case, ΔE_{elec} will no longer equal $\Delta E_{e\text{-field}}$. For example, when the polarity of ΔE_{in} is positive, which matches the polarity of the applied voltage (Scheme 1c), $\Delta E_{elec} < \Delta E_{e\text{-field}}$. In contrast, when the polarity of ΔE_{in} is negative, which opposes the polarity of the applied voltage (Scheme 1d), $\Delta E_{elec} > \Delta E_{e\text{-field}}$.

In the situation described by eq 2, the BPE enters an active mode, where a voltage applied directly to the BPE microbands plays a role in determining ΔE_{elec}. Because ΔE_{elec} is the driving force for electrochemical reactions at the BPE, manipulation of ΔE_{in} provides a means for controlling the rate of electrochemical reactions at the two poles of the BPE. Because ΔE_{in} is applied locally, many pairs of microband electrodes can be controlled independently of one another for a constant value of $\Delta E_{e\text{-field}}$. Importantly, the voltage source that applies ΔE_{in} need not be a power supply or battery, which are used for this purpose in the present study, but rather could be any electrochemical reaction that provides a suitable voltage.

Using Electrogenerated Chemiluminescence (ECL) as the Device Output. In this study, ΔE_{elec} is controlled by electrochemical logic gates, and the digital output is then reported by an optical ON/OFF signal rather than by an electrical signal. When $\sim$2.10 V > ΔE_{elec} > $\sim$1.60 V, O_2 will be reduced at the cathode[13] of the BPE and $Ru(bpy)_3^{2+}$ and TPrA will be oxidized at the anode, thus generating an ECL signal at the anodic pole.[19] The upper voltage limit is set by the onset of ECL quenching (see Supporting Information). The presence of ECL represents a digital "true", "high", or "1" output, while no ECL emission indicates a digital "false", "low", or "0" output. We will call the lower voltage threshold for ECL emission ΔE_{ECL}, and

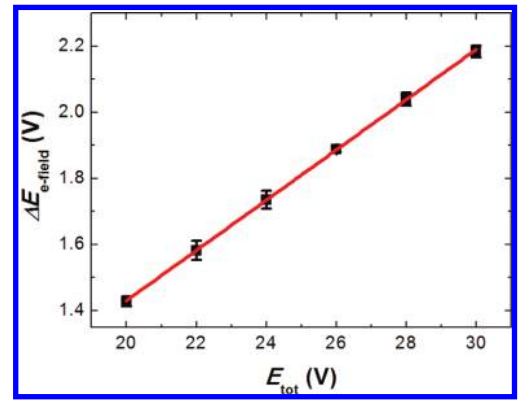
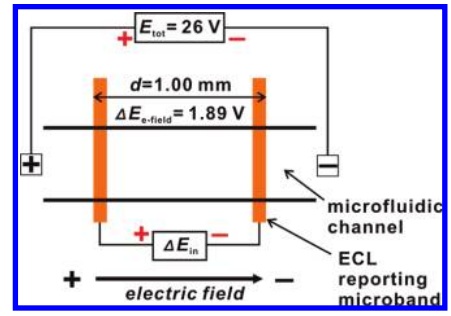


Figure 1. Plot of $\Delta E_{e\text{-field}}$, measured between two microbands (d = 1.00 mm), as a function of the driving voltage (E_{tot}).

Scheme 2



therefore when $\Delta E_{elec} > \Delta E_{ECL}$ (1.60 V), an ECL signal will be detected at the anodic pole of the BPE.

Determination of Input Parameters. The electric field (V_0) in the microfluidic channel is generated by a pair of driving electrodes placed in reservoirs at either end of the channel, and these electrodes supply a driving voltage (E_{tot}), as Scheme 1 illustrates. Therefore, $V_0 = E_{tot}/l_{channel}$, where $l_{channel}$ is the length of the microfluidic channel. However, the actual value of V_0 is always somewhat smaller than this equation predicts, because some of E_{tot} is lost at the driving electrode/solution interface.[19] For sensor applications,[13] we normally ignore this loss but it is not negligible in the logic gate calculations. Accordingly, accurate values of V_0 were measured by determining $\Delta E_{e\text{-field}}$ between two microband electrodes having a spacing of d = 1.00 mm, while E_{tot} was varied between 20.0 and 30.0 V. The results of this experiment are plotted in Figure 1. Using the values from this experimentally determined curve and eq 1 to substitute $V_0 d$ for $\Delta E_{e\text{-field}}$, we can write V_0 (V/mm) with d = 1.00 mm as a linear function of E_{tot} (eq 3).

$$V_0 = 0.076 \times E_{tot} - 0.089 \quad (3)$$

Using eqs 1−3, the value of ΔE_{in} required to turn a logic gate on or off can be reliably estimated. For example, the NOT gate shown in Scheme 2, with d = 1.00 mm and E_{tot} = 26.0 V, has an estimated ΔE_{elec} = 1.89 V (eq 3) when ΔE_{in} = 0 V; that is, when the input is "0". This value of 1.89 V is larger than the threshold potential for ECL (ΔE_{ECL} = 1.60 V), so ECL will be present and the NOT gate has a value of "1". To prevent ECL emission, so that the device output is "0", ΔE_{elec} must be < ΔE_{ECL}. This requires a voltage input ("1") across the BPE such that ΔE_{in} is large enough to force ΔE_{elec} < 1.60 V, as shown in Scheme 1c and eq 2. In other words, the input must satisfy: $\Delta E_{e\text{-field}} - \Delta E_{in} = \Delta E_{elec} < \Delta E_{ECL}$. For this example we find

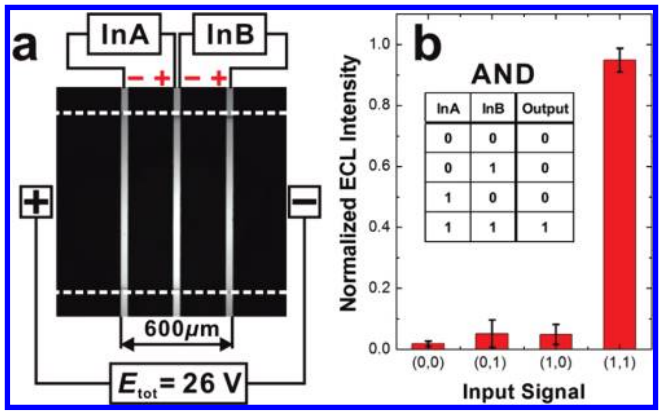


Figure 2. (a) Optical micrograph of an AND gate. The dashed white lines indicate the location of the microfluidic channel. Input signals are applied through InA and InB, which have the opposite polarity of the electric field. The microband electrode on the right is the anodic pole of the split BPE, and it reports the state of the device via ECL emission. (b) Normalized ECL intensities of the output signal as a function of the input voltages. The truth table for an AND gate is provided in the inset.

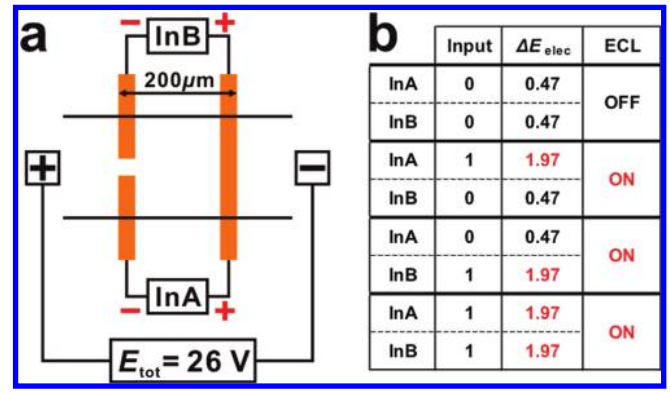


Figure 3. (a) Schematic diagram of the OR gate. Two input terminals are connected in parallel and share a common ECL reporting electrode. (b) The table provides values of ΔE_{elec}, estimated from eqs 5 and 6 and the applied input voltages, which correctly predict the ECL on/off state of the device.

that $\Delta E_{in} > \Delta E_{e\text{-field}} - \Delta E_{ECL} = 1.89 - 1.60 = 0.29$ V. The value 0.29 V, then, is the minimum value of ΔE_{in} that can act as the logic input "1" and prevent ECL emission. To summarize: an input of "1" will prevent ECL at the BPE, giving an output of "0", while an input of "0" will not disrupt the ECL signal, yielding an output of "1". This behavior is consistent with the truth table of a NOT gate.[5] Note that the value of ΔE_{in} required to change the output state of the logic gate depends strongly on $\Delta E_{e\text{-field}}$, which is a function of d, $l_{channel}$, and E_{tot}.

AND, OR, NAND, and NOR Logic Gates. Each of these four logic gates receives two input signals and sends one output signal, and here we demonstrate how a simple set of three microband electrodes can be designed to perform any of these logic functions.

An AND gate is constructed from three microbands spanning the width of the microchannel and spaced by 300 μm ($d = 600$ μm, Figure 2a). Two input terminals, InA and InB, are connected between the microbands in series to create a split BPE that can receive external voltage inputs. The input voltages used to control this device were supplied by a dual-output power supply with values for ΔE_{in} of 0 V for an input of "0" and -0.30 V for an input of "1". Note that these input voltages were applied with a polarity opposite that of the applied electric field, $E_{tot} =$ 26.0 V (Scheme 1d). The term for ΔE_{in} in eq 2 can now be expanded to accommodate two inputs (eq 4).

$$\Delta E_{elec} = \Delta E_{e\text{-field}} - \Delta E_{in,InA} - \Delta E_{in,InB} \quad (4)$$

Here, $\Delta E_{in,InA}$ and $\Delta E_{in,InB}$ are the components of ΔE_{in} from InA and InB, respectively. When InA = InB = 0 V, the measured voltage ($\Delta E_{e\text{-field}}$) between the two outer microband electrodes (Figure 2a) is 1.10 V (compare to the value calculated from eq 3, which is 1.13 V). Thus, an initial input of "0" to both InA and InB (0,0) results in $\Delta E_{elec} = 1.10$ V, according to eq 4. This value for ΔE_{elec} is less than the required voltage for ECL emission ($\Delta E_{ECL} = 1.60$ V); therefore, the ECL output will be "0". However, when input (1,1) is applied, ΔE_{elec} will increase to 1.70 V (eq 4), and this value is now higher than ΔE_{ECL} so that ECL is observed and the device output is "1". When either input (1,0) or (0,1) is applied, ΔE_{elec} will equal 1.40 V, which is still less than ΔE_{ECL}. Therefore, no ECL will be visible and the output will remain "0". The ECL intensities from a functional microelectrochemical AND gate are shown in Figure 2b, along with the AND truth table.

The OR logic gate was designed around parallel, rather than serial, connections between inputs InA and InB, where the anodic microband is the ECL emitter (Figure 3). Due to these parallel connections, ΔE_{elec} is affected equally by either input, as expressed in eqs 5 and 6.

$$\Delta E_{elec,InA} = \Delta E_{e\text{-field}} - \Delta E_{in,InA} \quad (5)$$

$$\Delta E_{elec,InB} = \Delta E_{e\text{-field}} - \Delta E_{in,InB} \quad (6)$$

Here, $\Delta E_{elec,InA}$ and $\Delta E_{elec,InB}$ are the voltages between each of the two shorter electrodes and the long electrode in Figure 3. For this system, $d = 200$ μm, $E_{tot} = 26.0$ V, and the measured $\Delta E_{e\text{-field}}$ is 0.47 V. When $\Delta E_{in} = 0$ V, the input is "0", and when $\Delta E_{in} = -1.50$ V, the input is "1". Again, the polarity of the voltage inputs run opposite to that of the electric field applied to the driving electrodes (Scheme 1d). According to eqs 5 and 6, an input of (0,0) results in $\Delta E_{elec,InA} = \Delta E_{elec,InB} = 0.47$ V. In this case both $\Delta E_{elec,InA}$ and $\Delta E_{elec,InB}$ are less than ΔE_{ECL}, so the ECL output will be "0". For inputs of (1,0) and (0,1), ΔE_{elec} increases to 1.97 V despite the fact that only a single input is set high. Because 1.97 V > ΔE_{ECL}, an ECL output of "1" results. For an input of (1,1), eq 5 shows that ΔE_{elec} will again equal 1.97 V and therefore gives rise to an ECL output of "1". A more detailed explanation about the interplay between the two input signals for the AND and the OR gates, and their effect on the ECL emission, is provided in the Supporting Information.

NOR and NAND logic gates have the same basic designs as the just-described AND and OR gates, but the distances between the microbands are different and the polarity of the input signals are reversed so that they align with the electric field in the microchannel (Scheme 1c). For both the NOR and NAND systems: $d = 1.00$ mm, $E_{tot} = 26.0$ V, and the measured $\Delta E_{e\text{-field}} = 1.89$ V. The input voltages are $\Delta E_{in} =$ 0 V for "0" and 0.50 V for "1".

Figure 4a shows the NAND gate design. Because InA and InB are connected to the output terminal in parallel, eqs 5 and 6 apply to the NAND gate. For input (0,0), $\Delta E_{elec,InA} = \Delta E_{elec,InB} = 1.89$ V, which is > ΔE_{ECL}, so an ECL signal will be emitted from the anodic microband and the device output is "1". For input (1,0), $\Delta E_{elec,InA} = 1.89 - 0.50 = 1.39$ and $\Delta E_{elec,InB} = 1.89 - 0 = 1.89$ V. Because the latter value is higher than ΔE_{ECL}, and because the reporting anodic pole is connected in

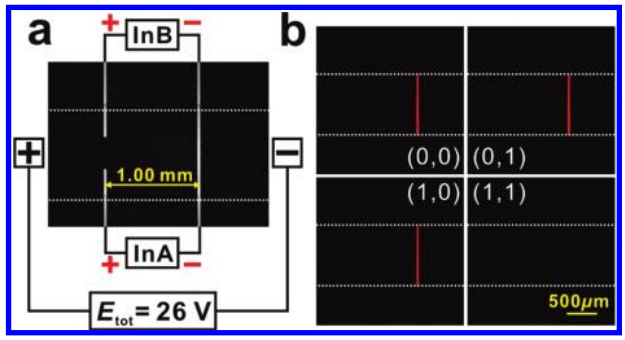


Figure 4. (a) Optical micrograph of a NAND gate showing the parallel configuration of the microband electrodes. The dashed white lines indicate the location of the microfluidic channel. (b) Luminescence micrographs of the output signals obtained using the four input signals indicated in parentheses. The ECL emission is shown in false color for clarity.

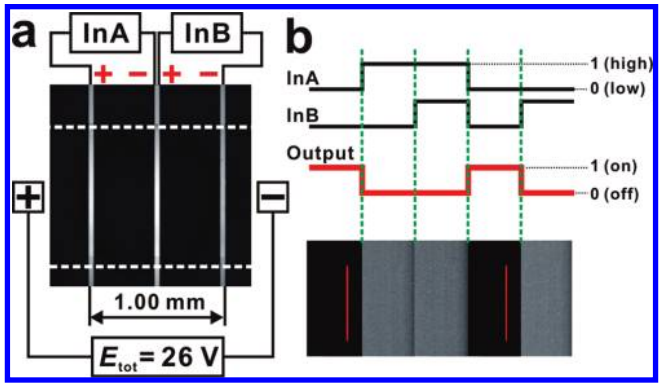


Figure 5. (a) Optical micrograph of a NOR gate. The dashed white lines indicate the location of the microfluidic channel. Input signals are applied through InA and InB, which have the same polarity as the electric field. (b) The logic operation was conducted with streaming input signals. InA and InB receive signals changing independently in the following order: (0,0) → (1,0) → (1,1) → (0,0) → (0,1). The ECL output is shown as a function of time in the luminescence micrograph.

parallel, the ECL signal will persist despite the fact that $\Delta E_{elec,InA}$ is $< \Delta E_{ECL}$. Consequently, an output of "1" is reported from an input of (1,0). The same reasoning applies for an input of (0,1), which also results in an output of "1". For input (1,1), the values of $\Delta E_{elec,InA}$ and $\Delta E_{elec,InB}$ are both 1.39 V, which is $< \Delta E_{ECL}$. The ECL signal is thus extinguished, yielding an output of "0". Figure 4b shows ECL micrographs of the output of a NAND gate operating under each of the four possible input configurations.

Figure 5a shows a NOR gate design, where the two input terminals are arranged in series, so that eq 4 applies. This system is similar to the AND gate design depicted in Figure 2, but the polarities of InA and InB are reversed. For input (0,0), ΔE_{elec} is calculated from eq 4 to be 1.89 V. This value is $> \Delta E_{ECL}$, and therefore ECL will be emitted to give an output of "1". For an input of either (0,1) or (1,0), ΔE_{elec} will equal 1.39 V, which is $< \Delta E_{ECL}$, so no ECL is generated and an output of "0" is reported. For input (1,1), $\Delta E_{elec} = 0.89$ V, and again no ECL is emitted. In summary, an output of "0" is reported for inputs of (0,1), (1,0), and (1,1), which is in keeping with the logic of the NOR operation. Figure 5b shows experimental output data for application of the following sequential input combinations: (0,0) → (1,0) → (1,1) → (0,0) → (0,1).

Integration of Multiple Logic Gates within a Microfluidic Channel. One of the main advantages of using BPEs in a microfluidic channel is that the uniform electric field acts identically on multiple electrodes. That is, if an array of BPEs

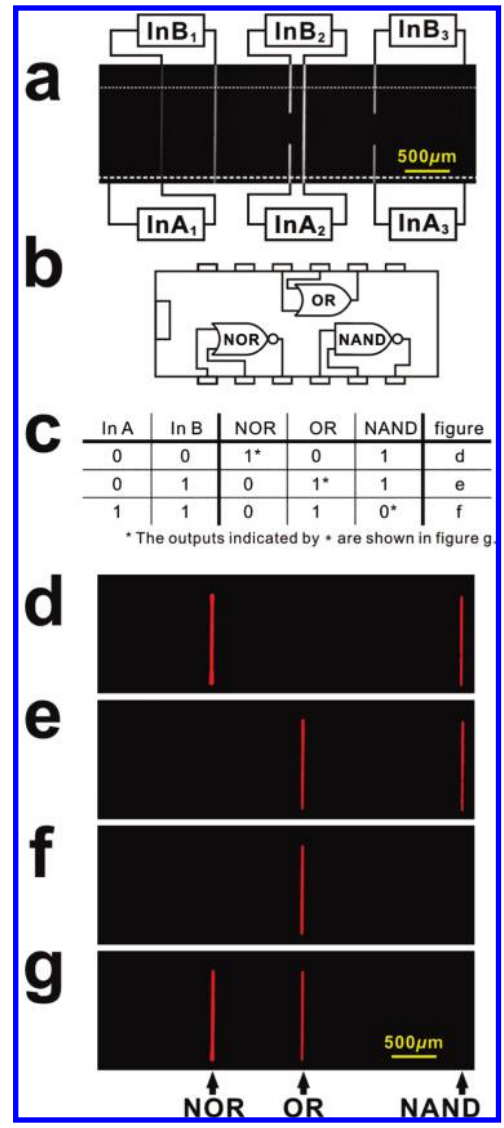


Figure 6. (a) Optical micrograph of an MIC composed of NOR, OR, and NAND logic gates (from left to right). (b) An equivalent electronic DIP-type IC. (c) The truth table for each logic gate. The output resulting from inputs of (0,0), (0,1), and (1,1), independently applied to each gate, is shown in luminescence micrographs d, e, and f, respectively. (g) Luminescence micrograph obtained with different input signals simultaneously applied to each logic gate: NOR (0,0); OR (0,1); NAND (1,1). The outputs marked with an asterisk in frame c correspond to the results in frame g.

is present in a single microchannel, each electrode will act independently of the others without the need for additional power supplies.[12,13] This property holds for split, as well as continuous, BPEs, and therefore it applies to the bipolar logic gate designs described here. Accordingly, an array of BPE logic gates can be easily fabricated and can operate in unison within a single microchannel. The efficacy of this idea is demonstrated in Figure 6a, where an array comprised of NOR, OR, and NAND gates operates simultaneously and independently within the same microchannel. This array can be thought of as a microelectrochemical integrated circuit (MIC) consisting of multiple signal operators. This configuration is akin to the electronic IC of dual in-line packages (DIPs) shown in Figure 6b. Each operator has two separate input terminals, so this IC can process six inputs simultaneously.

To demonstrate the function of this MIC, $\Delta E_{in} = 0$ V was used for an input of "0" and 1.5 V for an input of "1". The

power sources for these inputs were conventional AA batteries, which have a fixed output of 1.5 V. When input (0,0) was applied to all the logic gates, only the NOR and NAND gates reported output "1" (Figure 6d). When either input (0,1) or (1,0) was applied, an output of "1" was only observed at the OR and NAND gates (Figure 6e). When the input (1,1) was applied, only the OR gate reported an output of "1" (Figure 6f). These experimental results are summarized in the truth table shown in Figure 6c, where each logic gate has performed the proper algorithm.

Finally, to demonstrate the simultaneous and independent function of each logic gate, we applied different input signals to each of the logic gates in the array: (0,0) to NOR, (0,1) to OR, and (1,1) to NAND. The resulting outputs were "1", "1", and "0" (Figure 6g). This result perfectly matches the expected outputs denoted by asterisks in the truth table. Therefore, the electrochemical logic operators in the MIC responded correctly, individually, and simultaneously to their inputs.

Summary and Conclusions

The logic gates described here take advantage of bipolar electrochemistry in that they are powered without wires via a single pair of driving electrodes. This means they can operate as discrete devices or in an array format with little added complexity and no additional power supplies. In this paper we also introduced the concept of "active" BPEs and used them to construct individual and integrated logic gates. Under active control, the total potential difference between a BPE and the solution is supplied by a constant electric field through the microchannel as well as by a small external voltage applied directly across the microbands comprising the BPE. The external voltage source used here was a power supply or battery, but it could just as easily have been an unamplified electrochemical signal originating from a sensor or biological source.

As alluded to above, the input voltages used to activate these devices are small, ~1 V, while conventional electric control signals for TTL or CMOS range from 5 to 12 V. Indeed, the signal levels used in the logic designs described here are comparable to low-voltage-differential-signals (LVDS),[23] which are being developed for low-current applications in the electronics field. In addition, MICs are optoelectronic devices in that they accept electrical inputs and provide optical outputs. This is convenient, because it means that the state of the devices can be read without the need for wires.

Finally, an important aspect of the findings described here is the following. While the fluidic components of lab-on-a-chip devices are highly miniaturized, the data processing aspects have been largely ignored. Clearly, there is a place for self-powered, "sample-in−answer-out"[24] platforms, and the systems reported here are a first step in that direction. In the future, we anticipate full integration of data processing onto the chip, and that this will lead to interesting possibilities for smarter and more efficient chemical and biological sensors.

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Supporting Information Available: Additional information about ECL measurements as a function of applied potentials and about how the input signals affect the electrode potentials. This material is available free of charge via the Internet at http://pubs.acs.org.

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Supporting Information

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Design and Operation of Microelectrochemical Gates and Integrated Circuits

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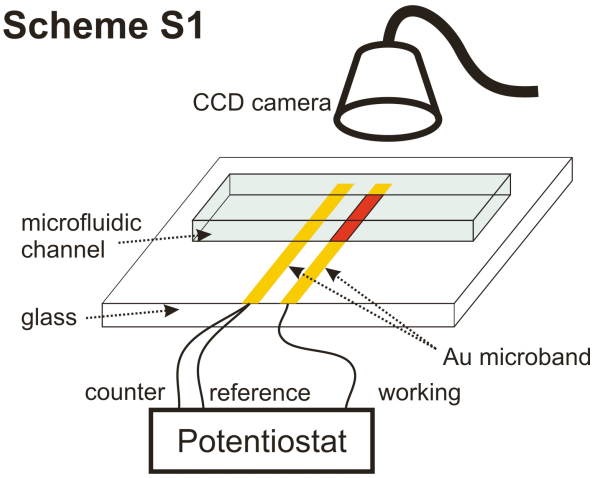
(5 pages)

Measurement of ΔE_{ECL}: the critical voltage for ECL. ECL reporting was used to report the output of the logic operations: near-zero emission for "0", and light emission for "1". ECL emission is the result of the electrochemical oxidation of $Ru(bpy)_3^{2+}$ and TPrA, which depends on the potential difference between the electrode and the solution. If the potential is too low, oxidation of these chemicals will not occur and ECL will not be emitted. If the potential is too high, the ECL pathway of $Ru(bpy)_3^{2+}$ and TPrA will be hindered by other reactions (for example, the oxidation of water or oxygen) that quench the ECL signal. Therefore, the optimal potential window for ECL must be determined.

By connecting two microbands in a microfluidic channel directly to a potentiostat, as shown in scheme S1, the ECL intensity could be determined as the potential difference (ΔE_{elec}) was modulated (in the absence of driving electrodes). The results can be dissected into three regions, as shown by the red vertical lines in Figure S1.

Scheme S1



Region (1) includes voltages below 1.45 V, region (2) is around 1.50 V, and region (3) includes voltages over 1.60 V. In region (1), no ECL was observed, so we can define this region as the digitized "0" signal. In region (3), clear and bright ECL was

observed, so this region can be defined as the digitized "1" signal. However, in region (2), between the "0" and "1" regions, a very low ECL intensity is observed, which may be closer to "0" than "1". Even though some ECL was observed below 1.60 V, it is more reasonable to define ΔE_{ECL} to be 1.60 V for a clear determination of the output.

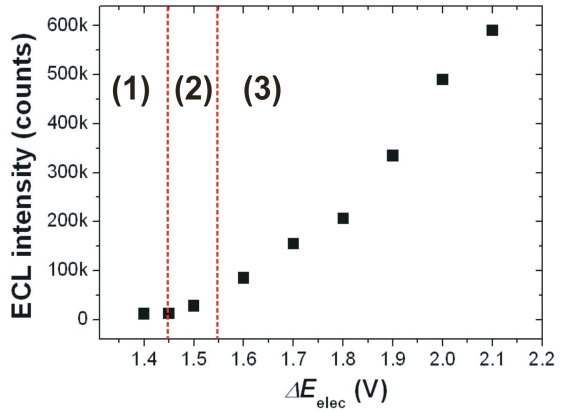


Figure S1. ECL intensities measured at different ΔE_{elec} values using the setup shown in Scheme S1.

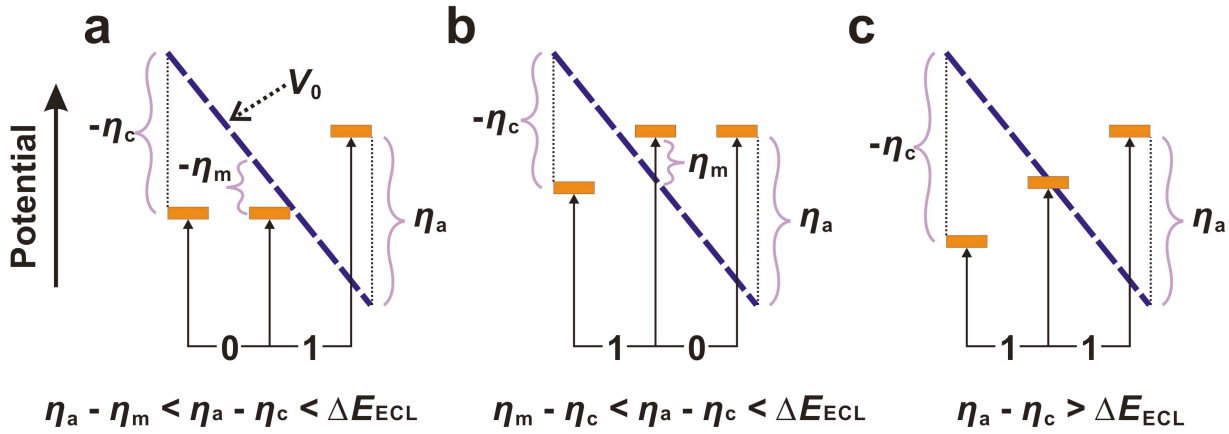
Schematic demonstration of potential change by two input signals

1. AND gate

In Figure 2 of the main text, three microband electrodes are connected in serial, but ΔE_{elec} is calculated as summation of potentials of only the outer electrodes ($\Delta E_{elec} = \eta_a - \eta_c$) regardless of the presence of the middle electrode. In Scheme S2, Frames a, b, and c illustrate the situation for inputs of (0,1), (1,0), and (1,1), respectively. Clearly, the potential differences between the middle electrodes and the solution (η_m) are much smaller than either η_a or $-\eta_c$, whether or not η_m is positive or negative. In other words, ΔE_{elec} for the middle electrode is $\eta_a - \eta_m$ (Scheme S2a) or $\eta_m - \eta_c$ (Scheme S2b), both of which are much lower than ΔE_{elec} of the outer electrodes, $\eta_a - \eta_c$.

As a result, electrochemistry on the middle electrode is thermodynamically inferior to the outer electrodes, and therefore the influence of the middle electrode on ECL emission from the AND gate is negligible. Consequently, the logic algorithm is only a function of ΔE_{elec} between the outer electrodes.

Scheme S2



2. OR gate

In Scheme S3a, the OR gate is composed of three microband electrodes connected in parallel, so that there can be two different potential states for ΔE_{elec}. When input (0,1) is applied to the OR gate in Scheme S3b, $-\eta_{c1}$ generated by input "1" is larger than $-\eta_{c2}$ generated by input "0". Consequently, ΔE_{elec} is dominated by input "1", and the value is $\eta_a - \eta_{c1}$.

Another complex configuration is illustrated in Scheme S3c. This situation is not probable, because the cathodic current

activated by a small amount of the negative potential ($-\eta_{c1}$) is hardly balanced with the anodic current by a large amount of the positive potential ($\eta_a + \eta_{c2}$), but it is still worth considering. Because the two electrodes on the left are connected through the right reporting electrode, the input voltage (ΔE_{in}) can polarize one of them anodic and the other cathodic, η_{c2} and $-\eta_{c1}$, respectively in the scheme. However, η_{c2} is much less than η_a as anode, so that bipolar electrochemistry will take place through the pathway of $\Delta E_{elec} = \eta_a - \eta_{c1}$, which is thermodynamically more favorable than the pathway of $\Delta E_{in} = \eta_{c2} - \eta_{c1}$. Experimentally, no ECL arising from η_{c2} was observed.

Scheme S3